Design In Reliability for communication Products

Uday B Reddy, Murty Dasaka, Pavan Kaipa

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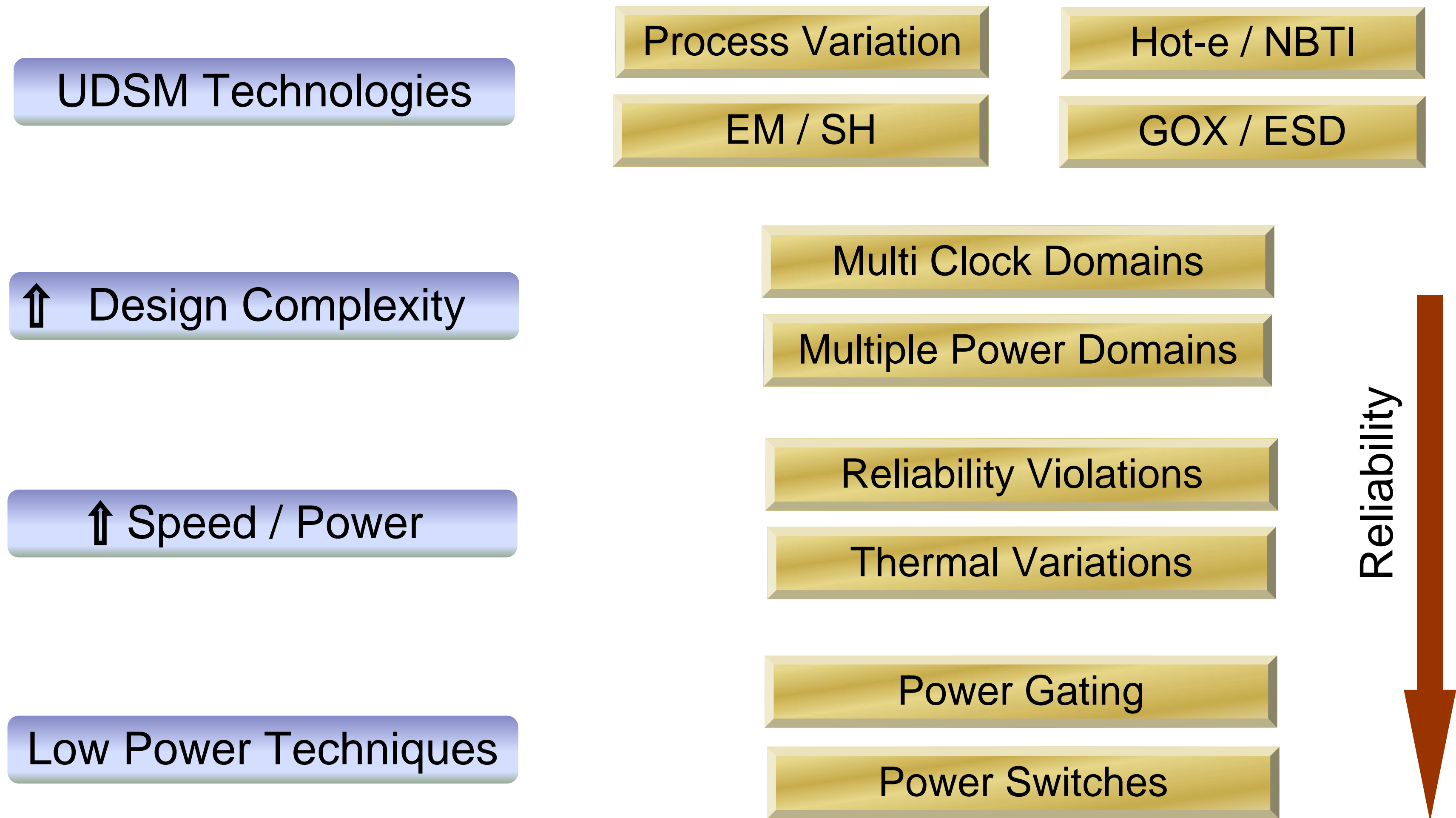
Intel Corporation

Agenda

- Introduction
- Design In Reliability (DIR) Challenges
- DIR Gaps/EDA Industry Requirements

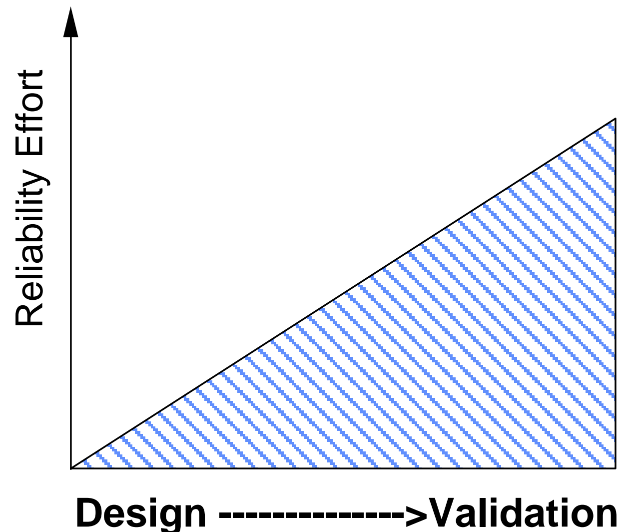
Introduction



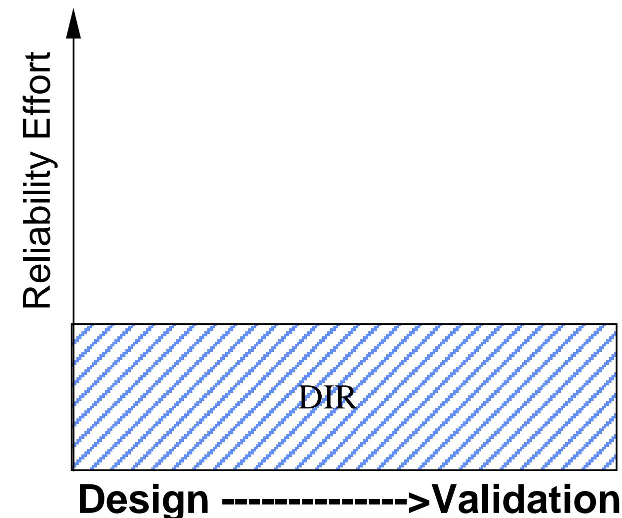
Technology/Design trends Impact Reliability negatively and is a major concern for getting robust products to consumers

DIR- Development trade-off

- Conventionally, Reliability verification was done in after-fact-design in the product design cycle.
  - With 65nm or below it is required to address it early in the design cycle to avoid significant rework.
- **Paradigm shift:**
  - Design In Reliability requires designers to keep reliability in mind with techniques like correct-by-construction.
  - EDA tools need to be enhanced to consider reliability rules and perform place/route to keep violations minimal.

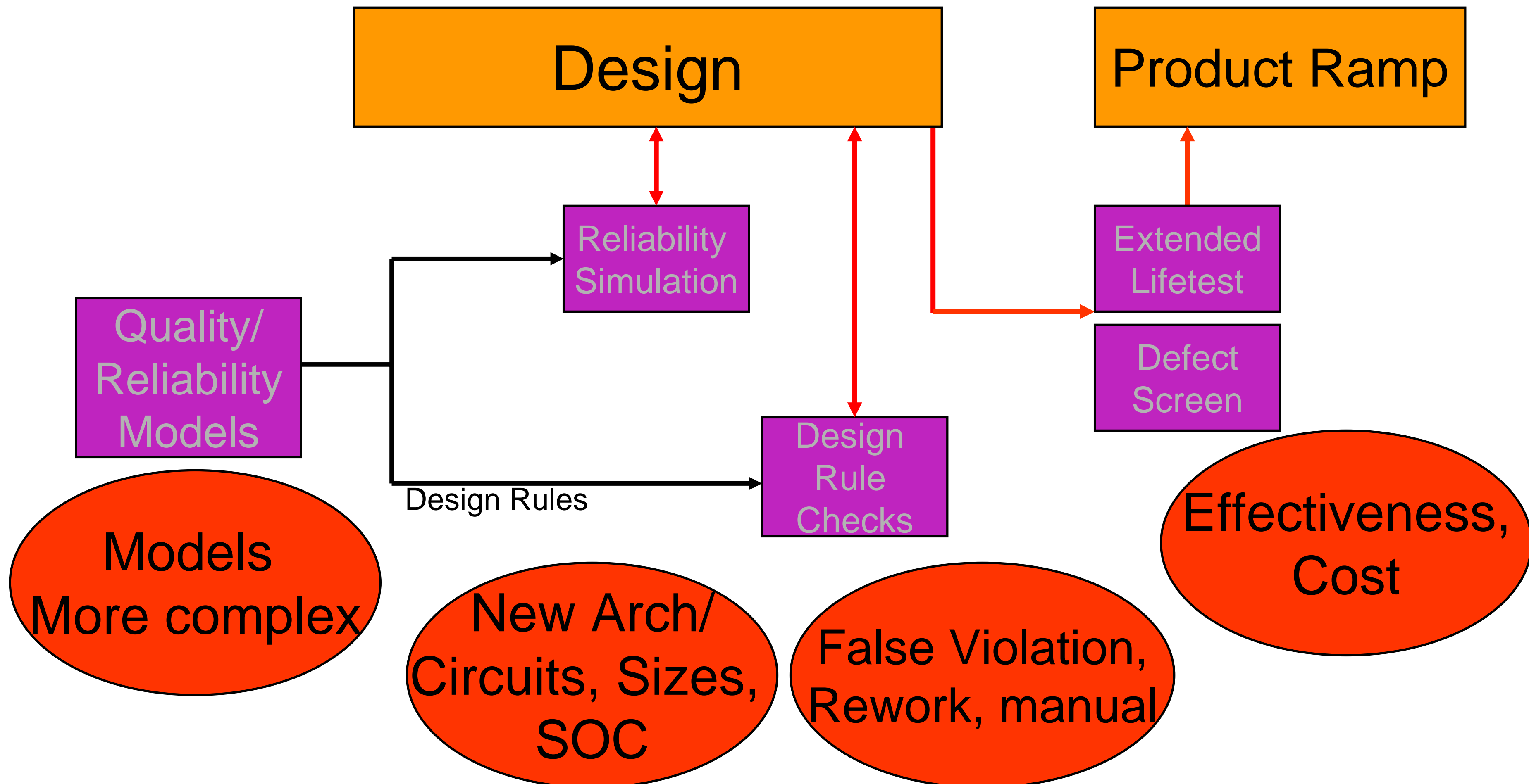


Old Technologies



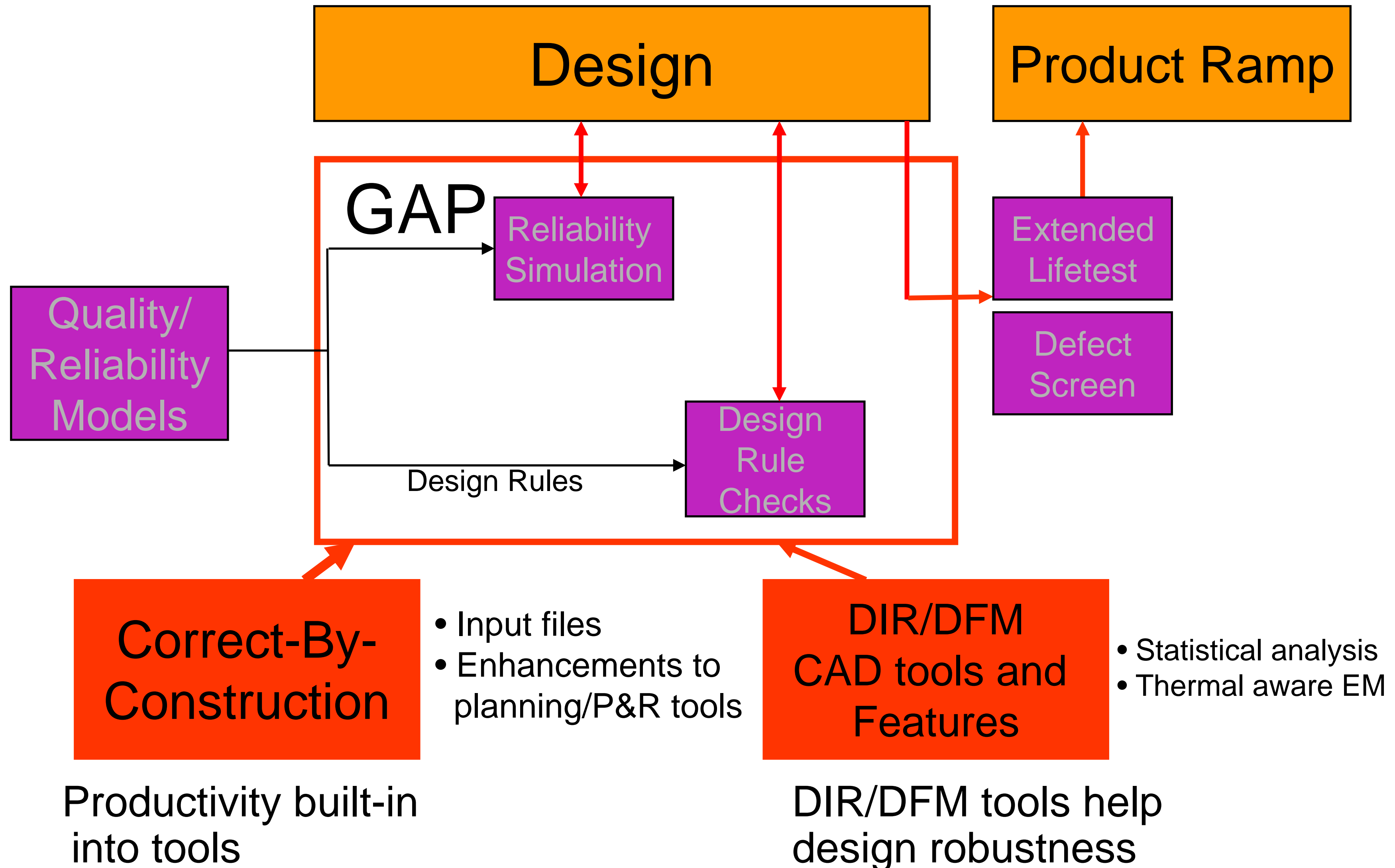
New Technologies

DIR Challenges



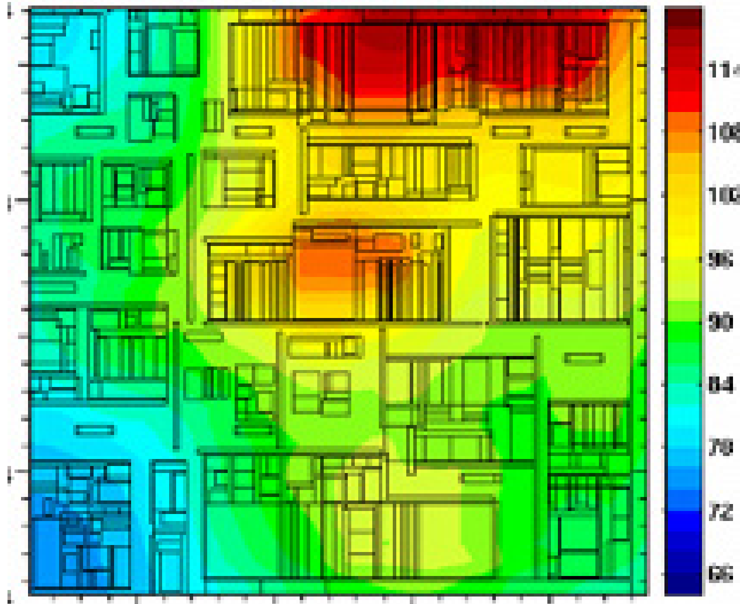
- Risk of having bad chips increasing rapidly

DIR GAPS



DIR Gaps in the EDA industry

Temperature aware Electro-migration and Self-Heat analysis.



Temperature dependence of Current Density limits

$T_{interconnect}$	Factor
80°C	3.92x
90°C	2.80x
100°C	2.00x
110°C	1.41x
120°C	1.00x
150°C	0.36x

- Fixing all the violations based on a fixed temperature (ex 120C) may not be realistic in 65nm and below.
- Applying local temperature based current density limits allows designers to waive false violations.

DIR Gaps in the EDA industry

Transient analysis of power domain during turn-on/off power switches

- Power Switch usage is getting common to meet the stand by power requirements.
- Turning-on power switches that supply to a huge block can cause transients in the global power network if turned on at once.
- Need to catch these transients early in the design to avoid costly silicon failures.
  - EDA tools are evolving in this area, but still immature.

DIR GAPS

- Statistical Variation
  - With the continued scaling of feature sizes, the ability to control critical device and interconnect parameters become increasingly difficult.
    - Intra-die random variations dominate inter-die random variation leading to designs not meeting specification
  - Parameters such as differential gain (in case of analog designs), delay (in case of digital designs) cannot be predicted precisely, rather can be predicted with in a confident interval
  - EDA tools are emerging to analyze the performance of the design in the presence of process variations.

DIR GAPS

- Statistical Variation
  - Analysis tools in Analog space (based on Monte Carlo Simulation) are more mature while tools in digital space to perform statistical timing analysis are still coming up.
    - As industry is moving towards 45nm it is important for these capabilities to get ready very soon
  - Tools for optimization are missing or less mature to enable robust designs in the presence of process variation.
    - Optimization tools required in both digital (cell based) and analog space
  - EDA tools to consider statistical variation of interconnect parameters are still evolving.

DIR GAPS

- ERC
  - Electrical Rule Checking at schematic design is used to identify pitfalls such as
    - Threshold voltage drops
    - Leakage
    - Charge Sharing
    - Crosstalk
    - Back-gate coupling
    - Minority carrier injection
    - Power Switching
  - No industry standard tools that are integrated with Schematic/ Layout design environment available
  - This is an important reliability requirement for 65nm or below designs

DIR Gaps in the EDA industry

- EM/SH checks on passive devices
  - Most of the RF blocks use inductors.
  - Almost all the existing EM/SH solutions treat inductors as ideal device and cannot check internal to the inductor layout.
  - Need tools to perform EM/SH analysis on inductors/poly resistors.
- Gate-Oxide (GOX) Failure analysis
  - Tools are needed to perform GOX failure analysis using over-shoot/ under-shoot information from Signal Integrity tools
- ESD Resistance check tools
  - ESD Rules exist to constrain the resistance between the clamps as well as clamp to diode.
  - Need tools to check for resistance between clamps and diodes at the full chip level.

Summary

- Deep submicron technology challenges & ever increasing design complexity creating a reliability risk for the products.
- Reliability Verification cannot be an after-fact-design, rather than in-design concept.
- EDA tools need to enable Design In Reliability for improved yield & reduce the product failure.
- Some Key Reliability gaps like *temp aware EM analysis, Transient Power grid analysis, Statistical variations, ESD* for sub 65nm design identified and discussed.